WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a pixel region;

a peripheral circuit region placed in at least a part of an area surrounding the pixel region;

gate electrodes of TFTs formed in the peripheral circuit region; and

a wiring connected to the gate electrodes and formed in a layer over or below the gate electrodes,

wherein the gate electrodes in different TFTs are isolated from one another.

2. A semiconductor device according to claim 1, wherein the wiring is a multilayer wiring having two or more layers.

3. A semiconductor device comprising:

a pixel region;

a peripheral circuit region placed in at least a part of an area surrounding the pixel region;

gate electrodes of TFTs formed in the peripheral circuit region; and

a short distance wiring connected to the gate electrodes and formed in a layer over or below the gate electrodes,

wherein the gate electrodes in different TFTs are isolated from one another.

4. A semiconductor device according to claim 3, wherein the short distance

wiring is a wiring led out in a pixel or a wiring for leading one functional block.

5. A semiconductor device according to claim 3, wherein the short distance wiring is 2 μm or longer and shorter than 2 cm.

6. A semiconductor device according to any one of claim 3, wherein the short distance wiring is a multilayer wiring having two or more layers.

7. A semiconductor device according to any one of claim 3, further comprising a long distance wiring that is formed in a layer over the short distance wiring.

8. A semiconductor device comprising:

a pixel region;

a peripheral circuit region placed in at least a part of an area surrounding the pixel region;

gate electrodes of TFTs formed in the peripheral circuit region; and

a long distance wiring formed in a layer over or below the gate electrodes,

wherein the gate electrodes in different TFTs are isolated from one another.

9. A semiconductor device according to claim 8, wherein the long distance wiring is hundred times longer than the pixel pitch, or more.

10. A semiconductor device according to any one of claims 8, wherein the long distance wiring is 2 cm or longer and shorter than 10 cm.

11. A semiconductor device according to any one of claim 8, wherein the long distance wiring is a multilayer wiring having two or more layers.

12. A semiconductor device according to claim 2, wherein at least one of the layers of the multilayer wiring is formed from a low resistance material.

13. A semiconductor device according to claim 6, wherein at least one of the layers of the multilayer wiring is formed from a low resistance material.

14. A semiconductor device according to of claim 11, wherein at least one of the layers of the multilayer wiring is formed from a low resistance material.

15. A semiconductor device according to claim 12, wherein the low resistance material is one or more materials selected from the group consisting of copper, a copper alloy, gold, a gold alloy, silver, and a silver alloy.

16. A semiconductor device according to claim 13, wherein the low resistance material is one or more materials selected from the group consisting of copper, a copper alloy, gold, a gold alloy, silver, and a silver alloy.

17. A semiconductor device according to claim 14, wherein the low resistance material is one or more materials selected from the group consisting of copper, a copper alloy, gold, a gold alloy, silver, and a silver alloy.

18. A semiconductor device according to claim 1,

wherein a transistor is formed in the peripheral circuit region, and

wherein a multilayer wiring having two or more layers is formed over the transistor.

19. A semiconductor device according to claim 3,

wherein a transistor is formed in the peripheral circuit region, and

wherein a multilayer wiring having two or more layers is formed over the transistor.

20. A semiconductor device according to claim 3,

wherein a transistor is formed in the peripheral circuit region, and

wherein a multilayer wiring having two or more layers is formed over the transistor.

21. A method of manufacturing a semiconductor device, comprising:

forming a driver circuit TFT in a driver circuit region over a substrate and a pixel TFT in a pixel region over the substrate; and

forming a first wiring over the driver circuit TFT, a second wiring over the first wiring, and a third wiring above the second wiring, and forming a first capacitor element over a drain region of the pixel TFT and a second capacitor element over the first capacitor element.

22. A semiconductor device comprising:

a driver circuit TFT formed in a driver circuit region over a substrate;

a pixel TFT formed in a pixel region over the substrate;

a first wiring formed over the driver circuit TFT;

a second wiring formed over the first wiring;

a third wiring formed over the second wiring;

a first capacitor element formed over a drain region of the pixel TFT; and

a second capacitor element formed over the first capacitor element.

23. A method of manufacturing a semiconductor device, comprising:

forming a driver circuit TFT in a driver circuit region over a substrate and a pixel TFT in a pixel region over the substrate;

forming a first interlayer insulating film over the driver circuit TFT and the pixel TFT;

forming a first contact hole in a portion of the first interlayer insulating film that is in the pixel region, the first contact hole being positioned over a drain region of the pixel TFT;

forming, from a first conductive film, a first wiring over a portion of the first interlayer insulating film that is in the driver circuit region, and forming a drain electrode in the first contact hole from the first conductive film;

forming a second interlayer insulating film over the first wiring, the drain electrode and the first interlayer insulating film;

forming a second contact hole in a portion of the second interlayer insulating film that is in the pixel region, the second contact hole being positioned over the first contact hole and the drain electrode;

forming a third interlayer insulating film over the second interlayer insulating film and in the second contact hole;

forming, from a second conductive film, a second wiring over a portion of the third interlayer insulating film that is in the driver circuit region, and forming a first capacitor electrode in the second contact hole from the second conductive film;

partially exposing the third interlayer insulating film at the bottom of the second contact hole by etching the first capacitor electrode;

forming a fourth interlayer insulating film over the second wiring, the first capacitor electrode, and the third interlayer insulating film;

forming a third contact hole in a portion of the fourth interlayer insulating film that is in the pixel region, the third contact hole being positioned over the second contact hole and the first capacitor electrode;

forming a fifth interlayer insulating film over the fourth interlayer insulating film and in the third contact hole;

partially exposing the drain electrode positioned under the bottom of the third contact hole by etching portions of the third and fifth interlayer insulating films that are at the bottom of the third contact hole; and

forming, from a third conductive film, a third wiring over a portion of the fifth interlayer insulating film that is in the driver circuit region, as well as forming a second capacitor electrode in the third contact hole from the third conductive film and electrically connecting the second capacitor electrode to the drain electrode,

wherein a first capacitor element and a second capacitor element are formed in the first through third contact holes, the first capacitor element being composed of the drain electrode, the third interlayer insulating film as a dielectric, and the first capacitor

electrode, the second capacitor element being composed of the first capacitor electrode, the fifth interlayer insulating film as a dielectric, and the second capacitor electrode.

24. A method of manufacturing a semiconductor device according to claim 23, wherein electrically connecting the second capacitor electrode to the drain electrode is followed by forming a sixth interlayer insulating film over the third wiring, the second capacitor electrode, and the fifth interlayer insulating film, and forming, over a portion of the fifth interlayer insulating film that is in the pixel region, a pixel electrode that is electrically connected to the second capacitor electrode.

25. A semiconductor device, comprising:

a driver circuit TFT formed in a driver circuit region over a substrate and a pixel TFT formed in a pixel region over the substrate;

a first interlayer insulating film formed over the driver circuit TFT and the pixel TFT;

a first contact hole formed in a portion of the first interlayer insulating film that is in the pixel region, the first contact hole being positioned over a drain region of the pixel TFT;

a first wiring formed from a first conductive film over a portion of the first interlayer insulating film that is in the driver circuit region;

a drain electrode formed in the first contact hole from the first conductive film;

a second interlayer insulating film formed over the first wiring, the drain electrode and the first interlayer insulating film;

a second contact hole formed in a portion of the second interlayer insulating

film that is in the pixel region, the second contact hole being positioned over the first contact hole and the drain electrode;

a third interlayer insulating film formed over the second interlayer insulating film and in the second contact hole;

a second wiring formed from a second conductive film over a portion of the third interlayer insulating film that is in the driver circuit region;

a first capacitor electrode formed in the second contact hole from the second conductive film;

a hole for partially exposing the third interlayer insulating film at the bottom of the second contact hole, the hole being formed in the first capacitor electrode;

a fourth interlayer insulating film formed over the second wiring, the first capacitor electrode, and the third interlayer insulating film;

a third contact hole formed in a portion of the fourth interlayer insulating film that is in the pixel region, the third contact hole being positioned over the second contact hole and the first capacitor electrode;

a fifth interlayer insulating film formed over the fourth interlayer insulating film and in the third contact hole;

a hole for partially exposing the drain electrode positioned under the bottom of the third contact hole, the hole being formed in portions of the third and fifth interlayer insulating films that are at the bottom of the third contact hole; and

a third wiring formed from a third conductive film over a portion of the fifth interlayer insulating film that is in the driver circuit region;

a second capacitor electrode formed in the third contact hole from the third conductive film electrically connected to the drain electrode,

wherein a first capacitor element and a second capacitor element are formed in the first through third contact holes, the first capacitor element being composed of the drain electrode, the third interlayer insulating film as a dielectric, and the first capacitor electrode, the second capacitor element being composed of the first capacitor electrode, the fifth interlayer insulating film as a dielectric, and the second capacitor electrode.

26. A semiconductor device according to claim 25, further comprising: a sixth interlayer insulating film formed over the third wiring, the second capacitor electrode, and the fifth interlayer insulating film; and a pixel electrode formed over a portion of the fifth interlayer insulating film that is in the pixel region and is electrically connected to the second capacitor electrode.